CLAIM AMENDMENT

Claims 1 to 6. (canceled)

7. (new) A time-interleaved delta-sigma modulator for converting an analog signal to a digital signal, comprising,

a plurality of channel blocks, which has different phase of clock frequency, each channel block consisted of a first adder, a second adder, and a comparator,

wherein, said first adder receives an input signal according to clock frequency of each channel block, and an n channel block output u_n of the first adder is transmitted to the first adder and the second adder of an n+2 channel block, and an n block output v_n of the second adder is transmitted to the second adder of an n+2 block, and an output y_n that passes an n block comparator is transmitted to the first adder and the second adder of an n+2 block, so that said modulator sequentially receiving output from each block comparator for generating a final output y.

8. (new) The time-interleaved delta-sigma modulator of claim 7, wherein a number of said channel blocks have an odd number N greater than or equal to five.

9. (new) The time-interleaved delta-sigma modulator of claim 8, wherein said number of channel blocks is N, a phase difference between the n channel block and n+1 channel block is 1/N times the clock frequency.

10. (new) A time-interleaved delta-sigma modulator for converting an analog signal to a digital signal, comprising,

a plurality of channel blocks, which has different phase of clock frequency, each

channel block consisted of a first adder, a second adder, and a comparator,

wherein, said first adder receives an input signal according to clock frequency of each channel block, and an n channel block output u_n of the first adder is transmitted to the first adder and the second adder of an n+4 channel block, and an n block output v_n of the second adder is transmitted to the second adder of an n+4 block, and an output y_n that passes an n block comparator is transmitted to the first adder and the second adder of an n+4 block, so that said modulator sequentially receiving output from each block comparator for generating a final output y.

11. (new) The time-interleaved delta-sigma modulator of claim 10, wherein a number of said channel blocks have an odd number N greater than or equal to nine.

12. (new) The time-interleaved delta-sigma modulator of claim 11, wherein said number of channel blocks is N, a phase difference between the n channel block and n+1 channel block is 1/N times the clock frequency.